Precision, Very Low Noise, Low Input Bias Current Operational Amplifier

AD8671

FEATURES

Very low noise: 2.8 nV/√Hz, 77 nV p-p
Wide bandwidth: 10 MHz
Low input bias current: 12 nA max
Low offset voltage: 75 μV max
High open-loop gain: 120 dB min
Low supply current: 3 mA per amplifier
Dual-supply operation: ±5 V to ±15 V
Unity gain stable
No phase reversal

APPLICATIONS

PLL filters
Filters for GPS
Instrumentation
Sensors and controls
Professional quality audio

PIN CONFIGURATIONS

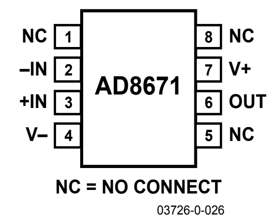

Figure 1. 8-Lead SOIC (R Suffix)

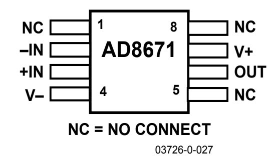

Figure 2. 8-Lead MSOP (RM Suffix)

GENERAL DESCRIPTION

The AD8671 is a very high precision amplifier featuring very low noise, very low offset voltage and drift, low input bias current, 10 MHz bandwidth, and low power consumption. Outputs are stable with capacitive loads of over 1000 pF. Supply current is less than 3 mA per amplifier at 30 V.

The AD8671's combination of ultralow noise, high precision, speed, and stability is unmatched, while the MSOP version requires only half the board space of comparable amplifiers.

Applications for these amplifiers include high quality PLL filters, precision filters, medical and analytical instrumentation, precision power supply controls; ATE, data acquisition, and precision controls as well as professional quality audio.

The AD8671 is specified over the extended industrial (–40°C to +125°C) temperature range.

The AD8671 is available in the 8-lead MSOP and 8-lead SOIC packages. Surface-mount devices in MSOP packages are available in tape and reel only.

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REVISION HISTORY

Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS, ±5.0 V

Table 1. V_S = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			20	75	μV
		−40°C < T_A < +125°C		30	125	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		0.3	0.5	μV/°C
Input Bias Current	I_B		−12	+3	+12	nA
		+25°C < T_A < +125°C	−20	+5	+20	nA
		−40°C < T_A < +125°C	−40	+8	+40	nA
Input Offset Current	I_{OS}		−12	+6	+12	nA
		+25°C < T_A < +125°C	−20	+6	+20	nA
		−40°C < T_A < +125°C	−40	+8	+40	nA
Input Voltage Range			−2.5		+2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −2.5 V to +2.5 V	103	120		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ , V_O = −3 V to +3 V	1000	6000		V/mV
Input Capacitance, Common Mode	C_{INCM}			6.25		pF
Input Capacitance, Differential Mode	C_{INDM}			7.5		pF
Input Resistance, Common Mode	R_{IN}			3.5		GΩ
Input Resistance, Differential Mode	R_{INDM}			15		MΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ, −40°C to +125°C	3.8	4.0		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ, −40°C to +125°C		−3.9	−3.8	V
Output Voltage High	V_{OH}	R_L = 600 Ω	3.7	3.9		V
Output Voltage Low	V_{OL}	R_L = 600 Ω		−3.8	−3.7	V
Output Current	I_{OUT}			±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4 V to ±18 V	110	130		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3	3.5	mA
		−40°C < T_A < +125°C			4.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		4		V/μs
Gain Bandwidth Product	GBP			10		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		77	100	nV p-p
Voltage Noise Density	e_n	f = 1 kHz		2.8	3.8	nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.3		pA/√Hz

ELECTRICAL CHARACTERISTICS, ±15 V

Table 2. V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			20	75	µV
		−40°C < T_A < +125°C		30	125	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		0.3	0.5	µV/°C
Input Bias Current	I_B		−12	+3	+12	nA
		+25°C < T_A < +125°C	−20	+5	+20	nA
		−40°C < T_A < +125°C	−40	+8	+40	nA
Input Offset Current	I_{OS}		−12	+6	+12	nA
		+25°C < T_A < +125°C	−20	+6	+20	nA
		−40°C < T_A < +125°C	−40	+8	+40	nA
Input Voltage Range			−12		+12	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −12 V to +12 V	103	120		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ , V_O = −10 V to +10 V	1000	6000		V/mV
Input Capacitance, Common Mode	C_{INCM}			6.25		pF
Input Capacitance, Differential Mode	C_{INDM}			7.5		pF
Input Resistance, Common Mode	R_{IN}			3.5		GΩ
Input Resistance, Differential Mode	R_{INDM}			15		MΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ, −40°C to +125°C	13.2	13.8		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ, −40°C to +125°C		−13.8	−13.2	V
Output Voltage High	V_{OH}	R_L = 600 Ω	11	12.3		V
Output Voltage Low	V_{OL}	R_L = 600 Ω		−12.4	−11	V
Output Current	I_{OUT}			±20		mA
Short Circuit Current	I_{SC}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4 V to ±18 V	110	130		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3	3.5	mA
		−40°C < T_A < +125°C			4.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		4		V/µs
Gain Bandwidth Product	GBP			10		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_{n\,p\text{-}p}$	0.1 Hz to 10 Hz		77	100	nV p-p
Voltage Noise Density	e_n	f = 1 kHz		2.8	3.8	nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.3		pA/√Hz

ABSOLUTE MAXIMUM RATINGS[1]

Table 3. AD8671 Stress Ratings

Parameter	Rating
Supply Voltage	36 V
Input Voltage	V_S– to V_S+
Differential Input Voltage	±0.7 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
RM, R Packages	–65°C to +150°C
Operating Temperature Range	
AD8671	–40°C to +125°C
Junction Temperature Range	
RM, R Packages	–65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec)	300°C

[1]Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 4. Package Characteristics

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
8-Lead MSOP (RM)	190	44	°C/W
8-Lead SOIC (R)	158	43	°C/W

[1]θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

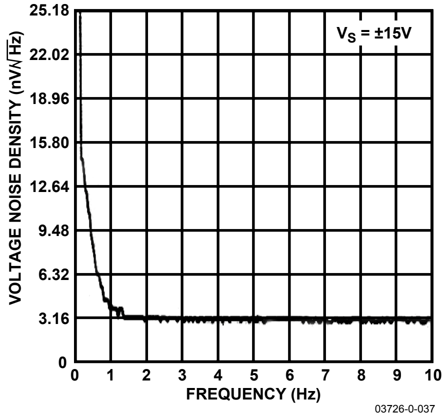


Figure 3. Voltage Noise Density vs. Frequency

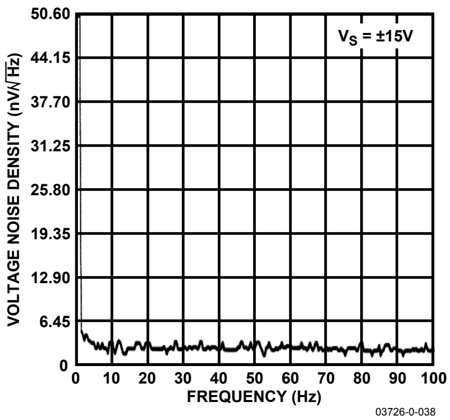


Figure 4. Voltage Noise Density vs. Frequency

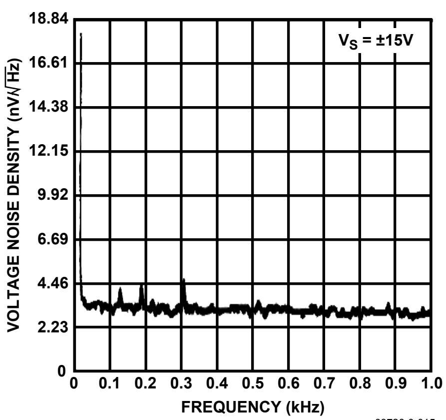


Figure 5. Voltage Noise Density vs. Frequency

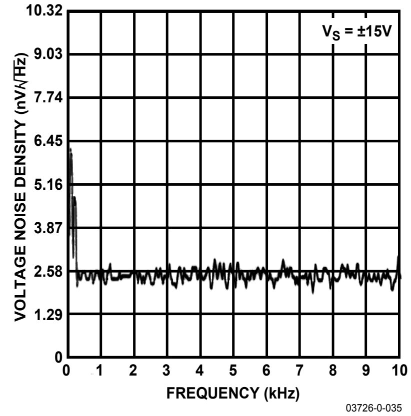


Figure 6. Voltage Noise Density vs. Frequency

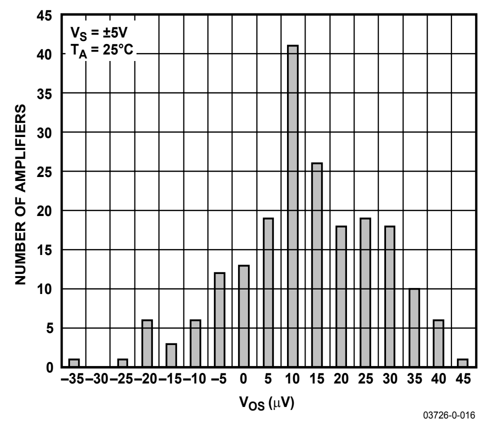


Figure 7. Input Offset Voltage Distribution

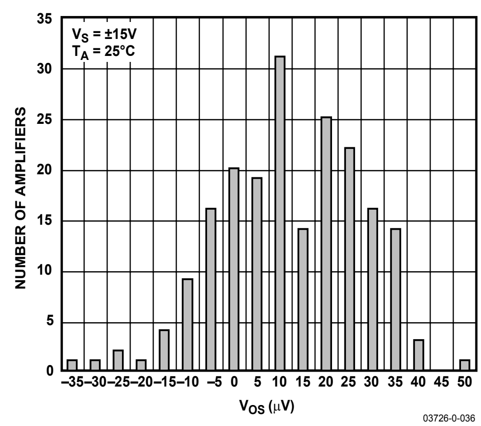


Figure 8. Input Offset Voltage Distribution

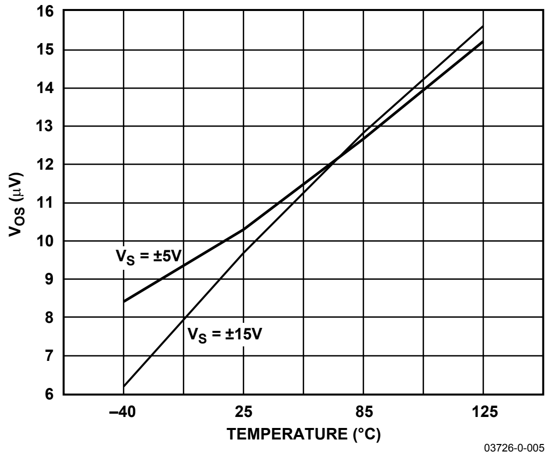


Figure 9. Input Offset Voltage vs. Temperature

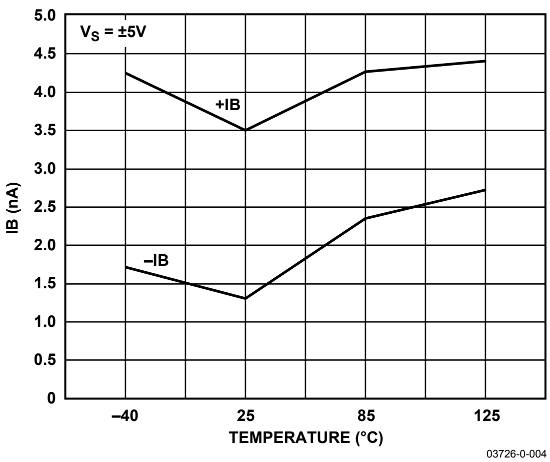


Figure 10. Input Bias Current vs. Temperature

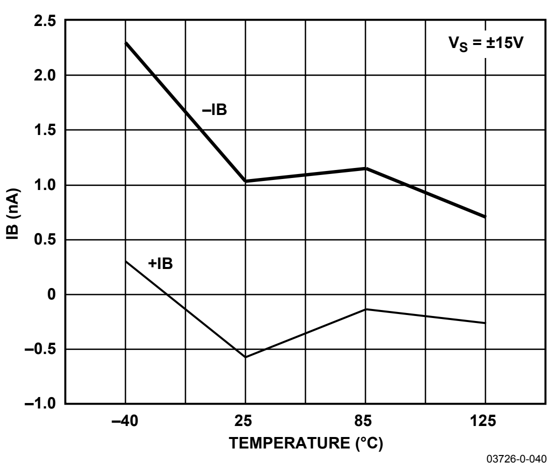


Figure 11. Input Bias Current vs. Temperature

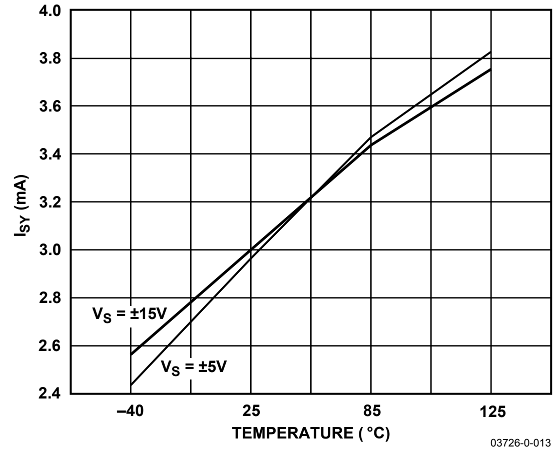


Figure 12. Supply Current vs. Temperature

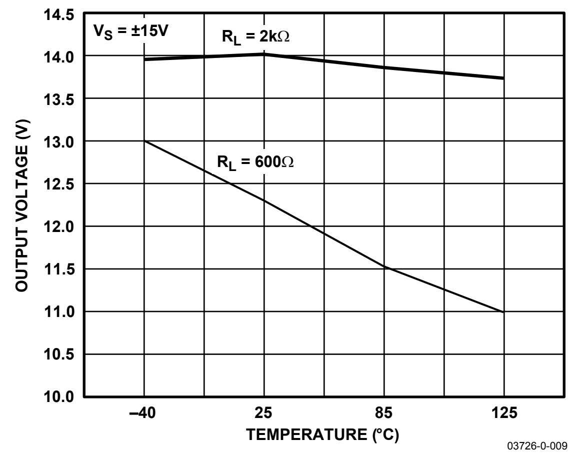


Figure 13. Output Voltage High vs. Temperature

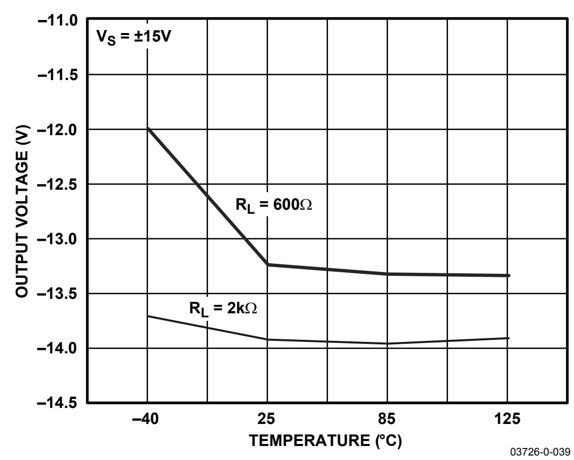


Figure 14. Output Voltage Low vs. Temperature

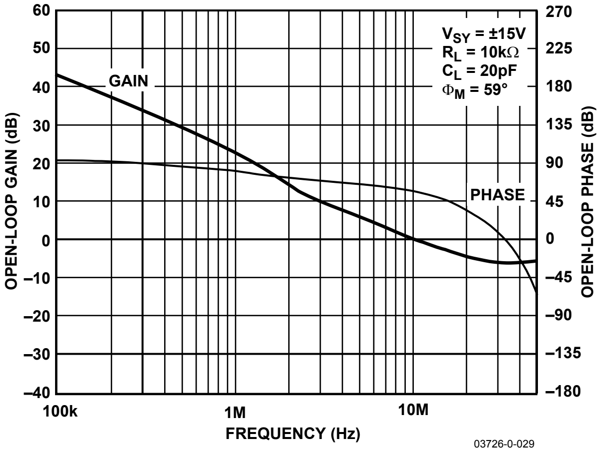


Figure 15. Open-Loop Gain and Phase Shift vs. Frequency

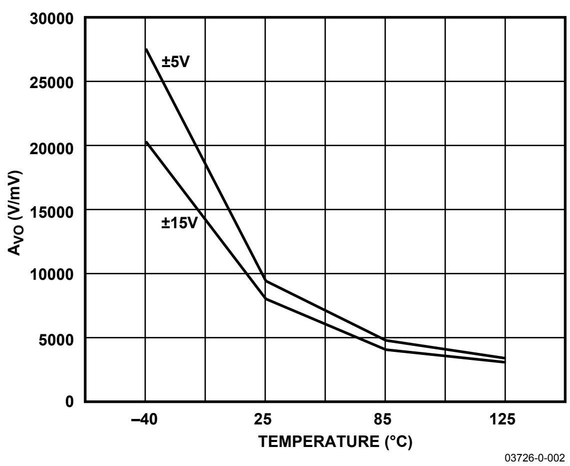


Figure 16. Open-Loop Gain vs. Temperature

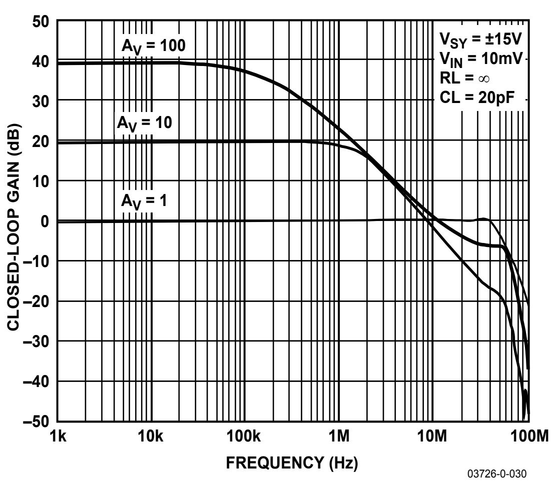


Figure 17. Closed-Loop Gain vs. Frequency

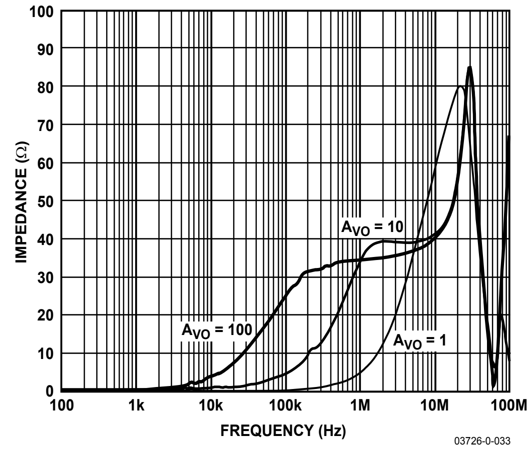


Figure 18. Output Impedance vs. Frequency

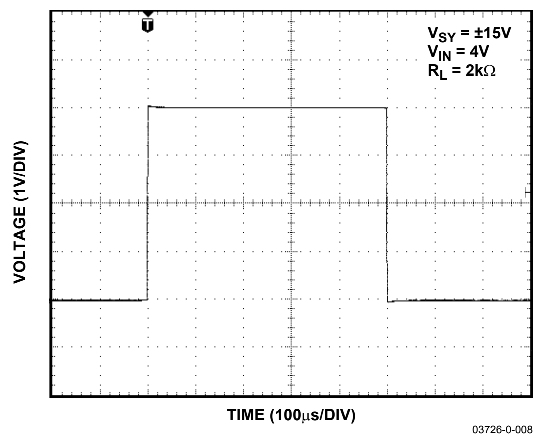


Figure 19. Large Signal Transient Response

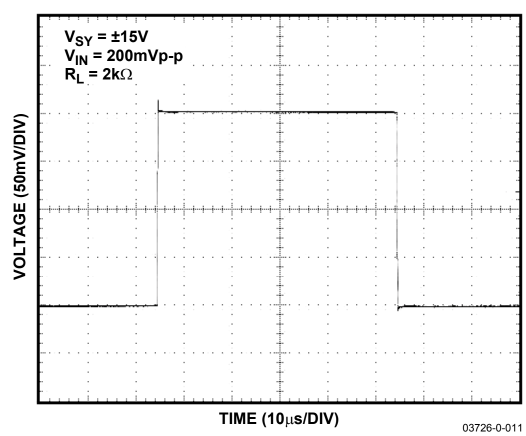


Figure 20. Small Signal Transient Response

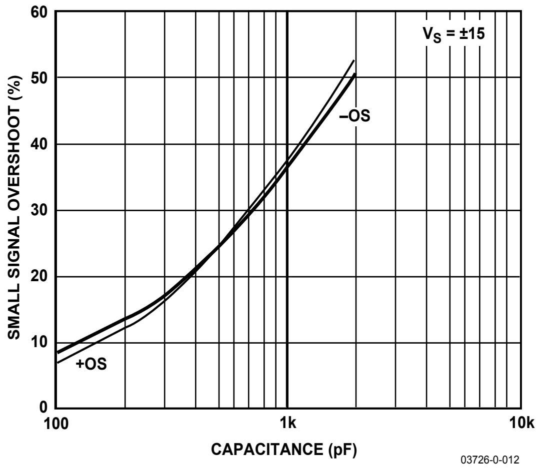


Figure 21. Small Signal Overshoot vs. Load Capacitance

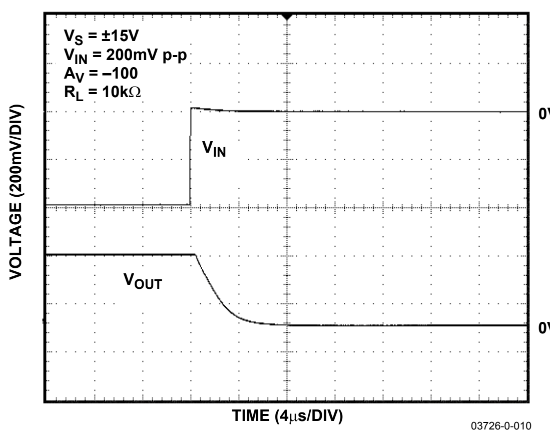


Figure 22. Positive Overdrive Recovery

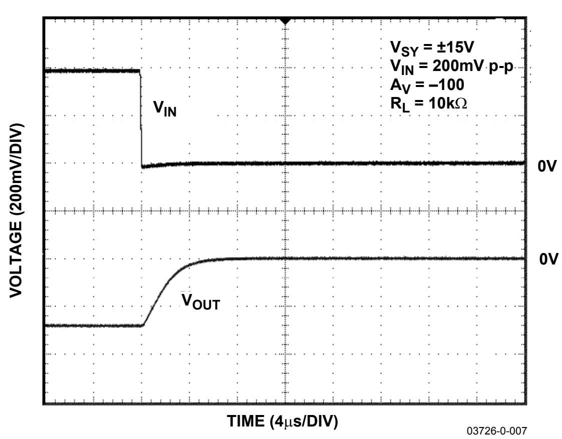


Figure 23. Negative Overdrive Recovery

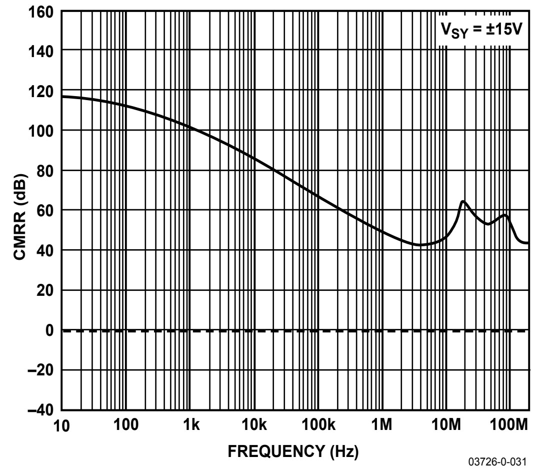


Figure 24. CMRR vs. Frequency

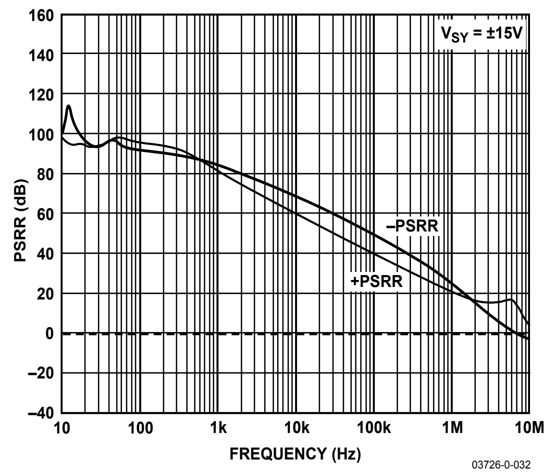


Figure 25. PSRR vs. Frequency

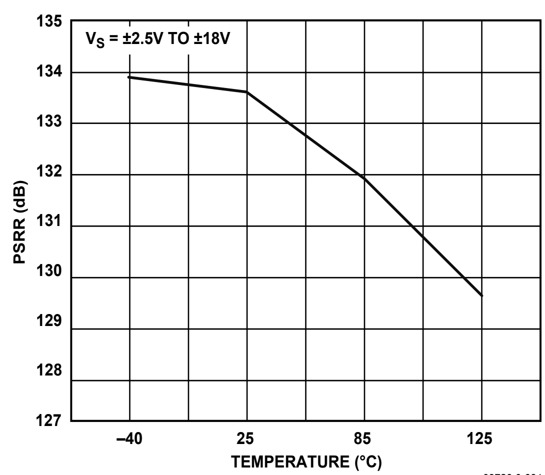


Figure 26. PSRR vs. Temperature

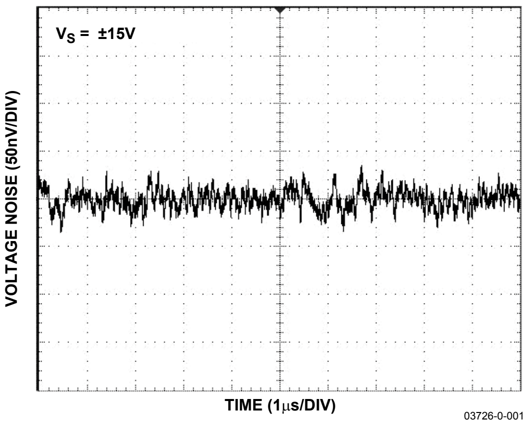


Figure 27. 0.1 Hz to 10 Hz Input Voltage Noise

APPLICATIONS

FOLLOWER APPLICATIONS

When large transient pulses (>1 V) are applied at the positive terminal of amplifiers (such as the OP27, LT1007, OPA227, and AD8671) with back-to-back diodes at the input stage, the use of a resistor in the feedback loop is recommended to avoid having the amplifier load the signal generator. The feedback resistor, R_F, should be at least 500 Ω. However, if large values must be used for R_F, a small capacitor, C_F, should be inserted in parallel with R_F to compensate for the pole introduced by the input capacitance and R_F.

Figure 28 shows the uncompensated output response with a 10 kΩ resistor in the feedback and the compensated response with C_F = 15 pF.

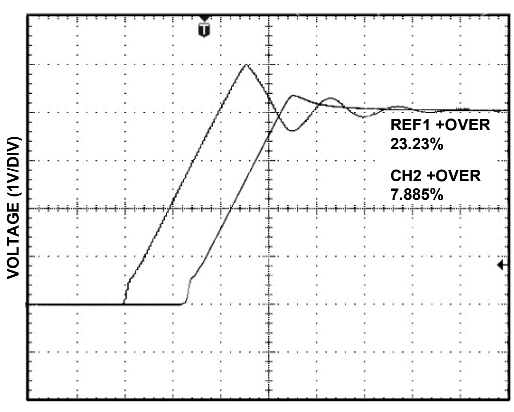


Figure 28. Transient Output Response

OUTPUT PHASE REVERSAL

Phase reversal is a change of polarity in the amplifier transfer function, which occurs when the input voltage exceeds the supply voltage. The AD8671 does not exhibit phase reversal even when the input voltage is 1 V beyond the supplies.

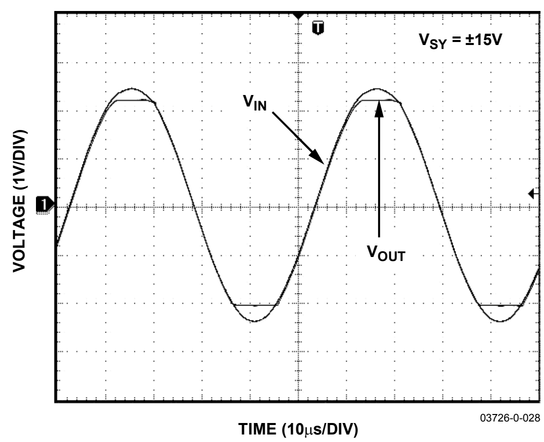


Figure 29. Output Phase Reversal

TOTAL NOISE VS. SOURCE RESISTANCE

The low input voltage noise of the AD8671 makes it a great choice for applications with low source resistance. However, because the AD8671 has low input current noise, it can also be used in circuits with substantial source resistance.

Figure 30 shows the voltage noise, current noise, thermal noise, and total rms noise of the AD8671 as a function of the source resistance.

For R_S < 475 Ω, the input voltage noise, e_n, dominates.
For 475 Ω < R_S < 412 kΩ, thermal noise dominates.
For R_S > 412 kΩ, the input current noise dominates.

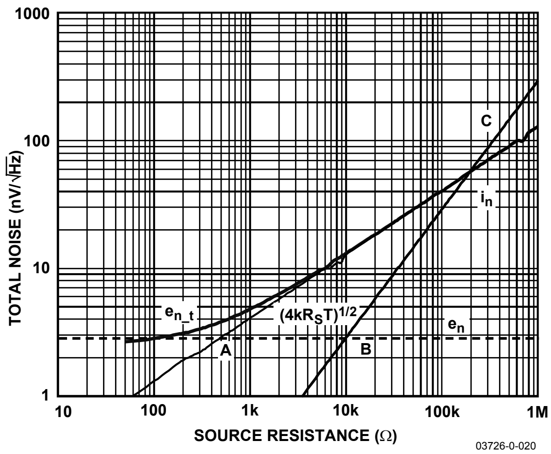


Figure 30. Noise vs. Source Resistance

THD + NOISE

The AD8671 exhibits low total harmonic distortion over the entire audio frequency range. This makes it suitable for applications with high closed-loop gains including audio applications. Figure 31 shows approximately 0.0006% of THD + N in a positive unity gain, the worst-case configuration for distortion.

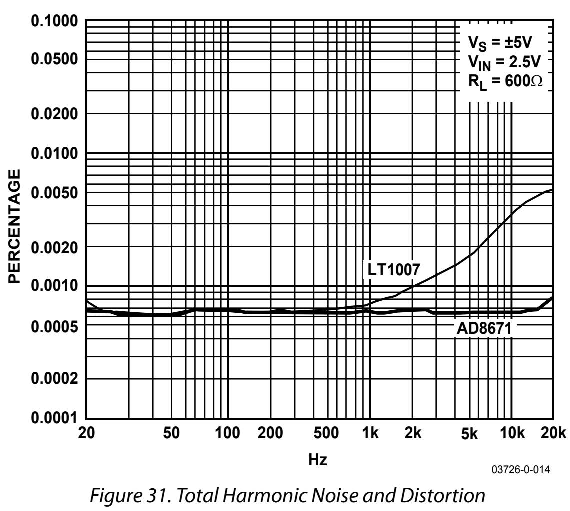


Figure 31. Total Harmonic Noise and Distortion

DRIVING CAPACITIVE LOADS

The AD8671 can drive large capacitive loads without causing instability. However, when configured in unity gain, driving very large loads can cause unwanted ringing or instability.

Figure 32 shows the output of the AD8671 with a capacitive load of 1 nF. If heavier loads are to be used in low closed-loop gain or unity gain configurations, it is recommended to use external compensation as shown in the circuit in Figure 33. This technique reduces the overshoot and prevents the op amp from oscillation. The trade-off of this circuit is a reduction in output swing. However, a great added benefit stems from the fact that the input signal as well as the op amp's noise are filtered, and thus the overall output noise is kept to a minimum.

The output response of the circuit is shown in Figure 34.

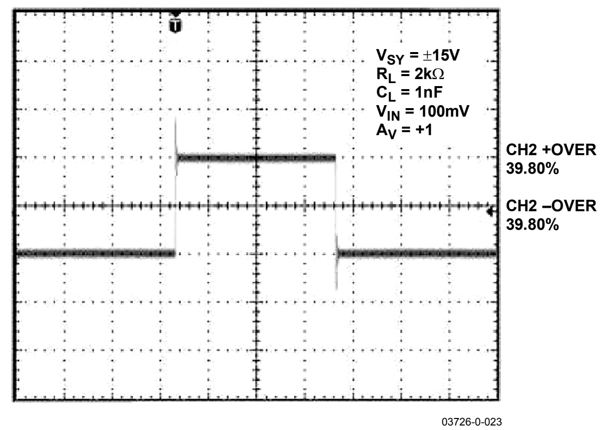


Figure 32. Capacitive Load Drive

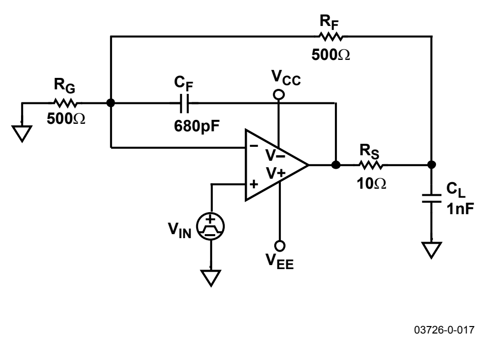


Figure 33. Recommended Capacitive Load Circuit

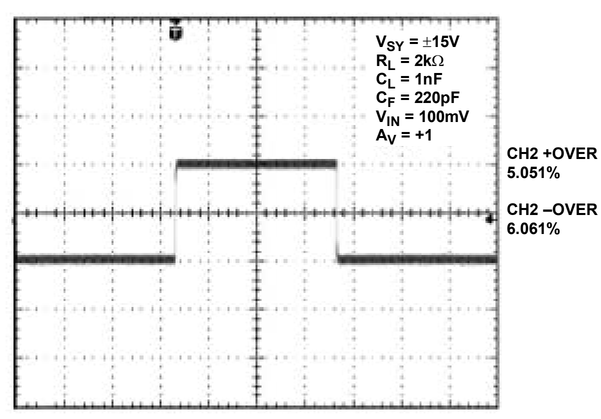


Figure 34. Compensated Load Drive

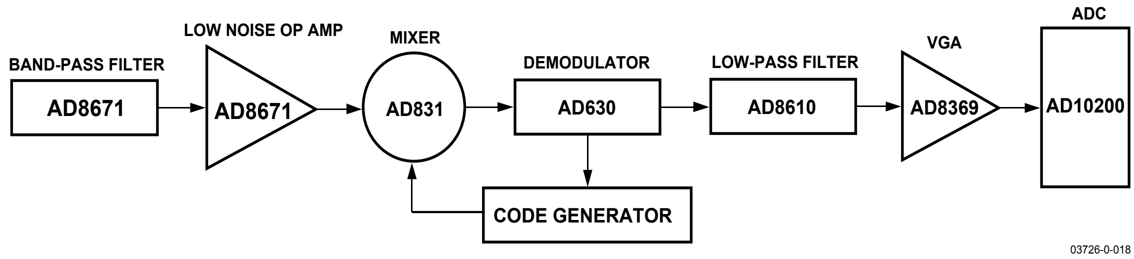


Figure 35. Simplified Block Diagram of a GPS Receiver

GPS RECEIVER

GPS receivers require low noise to minimize RF effects. The precision of the AD8671 makes it an excellent choice for such applications. Its very low noise and wide bandwidth make it suitable for band-pass and low-pass filters without the penalty of high power consumption.

Figure 35 shows a simplified block diagram of a GPS receiver. The next section details the design equations.

BAND-PASS FILTER

Filters are useful in many applications, for example, band-pass filters are used in GPS systems, as discussed in the previous section. Figure 36 shows a second order band-pass KRC filter.

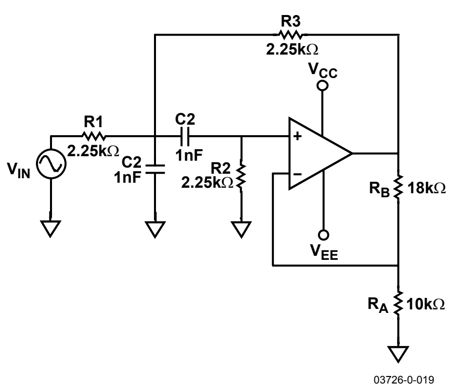


Figure 36. Band-Pass KRC Filter

The equal component topology yields a center frequency

$$fo = \frac{\sqrt{2}}{2\pi RC}$$

and $Q = \dfrac{\sqrt{2}}{4 - K}$

where:

$$K = 1 + \frac{R_B}{R_A}$$

The band-pass response is shown in Figure 37.

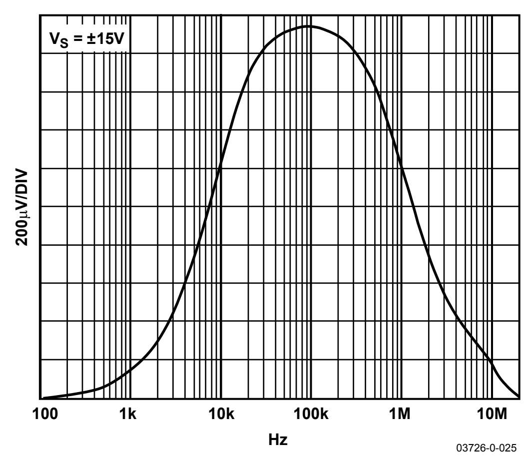


Figure 37. Band-Pass Response

PLL SYNTHESIZERS AND LOOP FILTERS

Phase-lock loop filters are used in AM/FM modulation.

Loop filters in PLL design require accuracy and care in their implementation. The AD8671 is an ideal candidate for such filter design; its low offset voltage and low input bias current minimize the output error. In addition to its excellent dc specifications, the AD8671 has a unique performance at high frequencies; the high open-loop gain and wide bandwidth allow the user to design a filter with a high closed-loop gain if desirable. To optimize the filter design, it is recommended to use small value resistors; this minimizes the thermal noise. A simple example is shown in Figure 38.

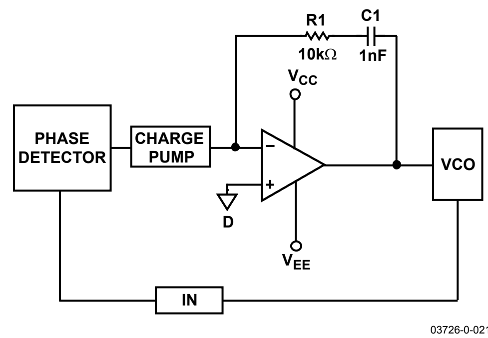
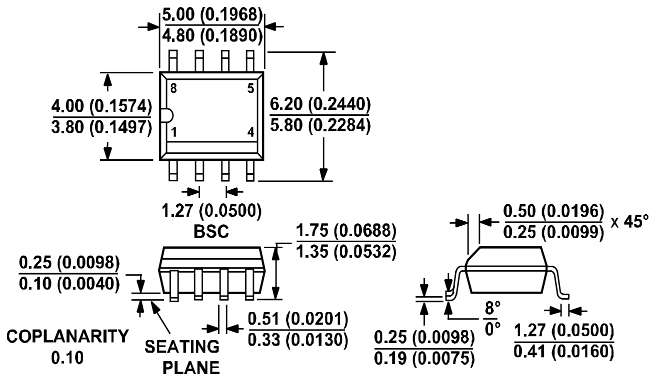


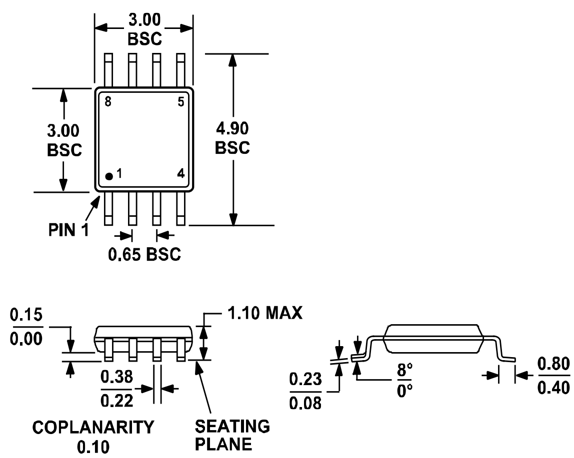
Figure 38. PLL Filter Simplified Block Diagram

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 39. 8-Lead SOIC Package



COMPLIANT TO JEDEC STANDARDS MO-187AA

Figure 40. 8-Lead MSOP Package
Dimensions in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8671AR-REEL	–40°C to +125°C	8-Lead SOIC	R-8	
AD8671AR-REEL7	–40°C to +125°C	8-Lead SOIC	R-8	
AD8671AR	–40°C to +125°C	8-Lead SOIC	R-8	
AD8671ARM-R2	–40°C to +125°C	8-Lead MSOP	RM-8	BGA
AD8671ARM-REEL7	–40°C to +125°C	8-Lead MSOP	RM-8	BGA

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